**Homework1: Introduction to Verilog HDL, Encoder, Counter**

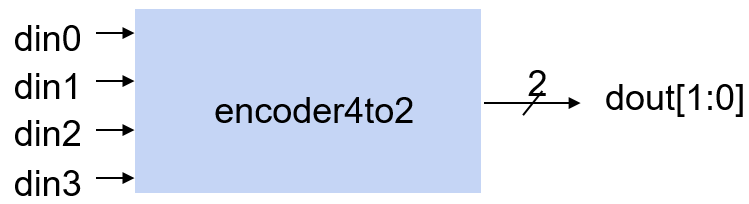
**Issued:** March 04 (Fri.), 2022 **Due:** March 09 (Wed.), 2022

**What to turn in**: Copy the text from your codes and paste it into a document. If a question asks you to plot or display something to the screen, also include the plot and screen output your code generates. Submit either a \*.doc or \*.pdf file.

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**Problem 1 (15p): Encoder**

Design a 4-to-2 encoder in Verilog. Please see the description in the lecture note

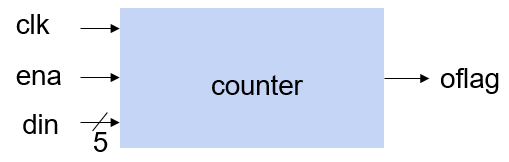


What you have to do:

* Design an encoder and its test bench based on the baseline codes.
* Submit your RTL files (encoder4to2.v and encoder4to2\_tb.v)
* Capture the waveform.

**Problem 2 (15p): Counter**

Design a down counter in Verilog. Please see the description in the lecture note



What you have to do:

* Design a down counter and its test bench based on the baseline codes.
* Submit your RTL files (counter.v and counter\_tb.v).
* Capture the waveform.

**Problem 3 (2p) (Optional): Bonus**

1. What is the clock frequency used in Problem 2? Change the clock frequency to 50MHz, do simulation again and capture the new waveform.
2. To update the internal counter in Problem 2, can we change the logic order (a) to (b)? Show a test case and its waveform to distinguish the logics (a) and (b).

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